CoreSim™ Design Analysis

Your ability to provide innovative products and services faster and more efficiently than your competitors is what sets you apart. Celestica’s CoreSim design analysis services can help you get to market first, reduce your development costs and improve your overall product quality.

Today’s rapidly advancing technology presents an increasingly complex set of problems to board designers in several areas – Design Complexity, High Speed Interfaces & Power Distribution. Design and compatibility issues not identified and addressed in the design phase will cause extended delays in time-to-market, increased development and opportunity costs, and decreased product quality and production yields.

The Celestica Solution
Celestica’s CoreSim suite of services uses specialized techniques to identify and resolve functional and parametric errors during the schematic entry & layout process. Our experienced engineering team leverages four complementary design analysis tools – Schematic Modeling, Signal Integrity Analysis, Board Static Timing Analysis and Power Integrity Analysis – to help our customers address design challenges as early in the product lifecycle as possible, assuring an optimal product design prior to first prototype arrival.

Celestica’s attention to detail, responsiveness to schedule requirements and deterministic analysis results are combined to provide timely and accurate guidance for our customers, helping them realize highly significant improvements to the board design process.

Delivering Competitive Advantage
Celestica’s CoreSim advanced design analysis service accelerates our customers’ design process while assuring high quality at lower costs.

- Reduces product development cost by eliminating costly re-spins
- Increases design efficiency by identifying issues earlier in the process
- Speeds time-to-market by streamlining design and prototyping
- Delivers higher production yields and product reliability by ensuring optimized product design
- Enables engineering resources to focus on core architecture and design

Schematic Modeling
CoreSim Schematic Modeling is a custom design validation service which uses Celestica’s proprietary tool and process to automate schematic checking on frequently encountered and hard-to-detect defects. This analysis and validation process is performed near the end of the schematic capture phase, greatly increasing the likelihood of single-pass PCB design success.

Utilizing a combination of automated tool and manual checks, schematic modeling complements existing human design reviews to offer early detection of functional/reliability issues, shorten layout and lab debug time and reduce design re-spin time. A comprehensive, customized report clearly identifies where errors are found, and provides recommended corrective actions.

This technique can be applied to schematics of any size, and to multiple interdependent schematics seen in multi-PCB products, including full system level analysis. A quick re-analysis is performed just prior to layout gerber release, ensuring that corrections and last minute additions to your schematics did not introduce any new defects into the design.

Signal Integrity Analysis
Analysis of analog effects on digital signals is now critical to all modern digital designs. Our Signal Integrity Analysis offering is comprised of three different types of analysis – Channel, Interconnect and Cross-Talk. Channel Analysis verifies that high-speed links (SRIO, PCIe, SAS, SATA) can meet the required bit error rates, while Interconnect Analysis verifies that the system interconnect is compliant to specification (i.e. PCIe, SAS, SATA), and Cross-Talk Analysis verifies that on-board signals do not interfere with each other, resulting in hard-to-debug intermittent problems.

By leveraging Signal Integrity Analysis, we can define accurate pre-layout constraints and ensure that your design is to specification, while automated feedback of flight time into the timing tool avoids yield/reliability issues. Additionally, SI Analysis also optimizes FPGA I/O buffer slew rate and drive strength, and optimizes signal quality to limit noise and radiated emissions.
CoreSim Design Analysis

Board Static Timing Analysis
The CoreSim custom board timing tool gives accurate pre-layout constraints and post-layout timing margins. The process checks device-to-device interface timing to provide layout constraints and to ensure board design is "right the first time", with centered timing margins using a custom Static Timing Analysis tool.

Pre-layout analysis is conducted before layout is complete, and provides topology, routing recommendations and constraints for optimum signal integrity and timing. Post-layout analysis commences after the board routing is complete – all nets in the interface are analyzed with back annotated signal integrity flight times to ensure that the routed board meets all timing requirements and constraints. Defining accurate pre-layout constraints and understanding worst-case timing margins helps to improve yields and reliability on boards.

Power Integrity Analysis
Verification of power distribution and related issues is achieved with our Power Integrity Analysis. Using simulation and verification tools, we are able to optimize decoupling capacitor quantity, value and placement to ensure sufficient power delivery to all devices on all DC rails.

With this advanced frequency-domain analysis, we can ensure that DC voltage droop at device power pins falls within specifications, that current density on traces and vias is within current carrying limits, and that voltage ripple at device power pins remains within tolerances.

By engaging with our engineers for Power Integrity Analysis, customers achieve lowest possible noise on power rails, capacitor optimization for value, count and placement, fewer complex power issues and high reliability.

Case Study: Reliability Issues in Existing Optical Transmission Product Family
Celestica's CoreSim design analysis suite finds the root causes for reliability issues in an existing metro optical transmission product line with a multi-service platform for a Tier One Telecom OEM.

Challenge:
High field failure rates for the product family were impacting customer satisfaction and product credibility. Upon inspection, many of the issues at the system level were believed to be complex marginality interactions at the board level, which made diagnostics and root cause identification difficult in the lab. In addition, the product family was built primarily through several acquisitions over a number of years. As such, the original design team was not available to support the root cause analysis and corrective actions. In all, 19 complex boards were suspected of creating the majority of the quality issues.

Solution:
Celestica’s engineering team engaged all four CoreSim solutions from our suite of services to analyze the suspect boards. The team suggested a baseline analysis of each board to eliminate the board level marginality. Schematic modeling looked at DC and connectivity, Signal Integrity/Static Timing looked for analog effects and timing on signals, and Power Integrity analysis checked for power issues.

Results:
On average, two major issues were identified on each suspect board. Based upon these findings, the customer was able to re-design four of the boards and alter the BOM on several other boards to remedy the problem. In addition, the board modeling was reusable for future changes. As a result, the customer saved an estimated $3 million in costly quality issues, and was able to dramatically improve customer satisfaction.

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